I2C BUS PROTOCOL DESIGN

1. Overview I2C bus protocol

a. Feature.

I2C BUS PROTOCOL

FSM I2C SLAVE

START

GENERATE

FSM I2C MASTER

CLOCK   
DIVIDE

b. Block diagram.

TOP MODULE

I2C PROTOCOL BUS

clk\_ex

rst\_n sda\_o

[1:0] address scl

[7:0] idata

[7:0] odata sda\_i

cs

rd

wr

c. Inputs / Outputs pin.

- Input :

* clk\_ex : clock of CPU.
* rst\_n : reset negedge of CPU.
* [1:0] address : 7 bit of address (I2C Slave).
* [7:0] idata : 8 bit of input data.
* cs : chip select posedge.
* rd : read posedge.
* wr : write posedge.
* sda\_i : serial data for read.

- Ouput :

* sda\_0 : serial data for write.
* scl : serial clock.

d. Register specifiaction.

2. START GENERATE.

a. Inputs / Outputs pin.

- Inputs :

* clk : clock internal.
* rst\_n : reset negedge from external.
* rd : signal read from bus.
* wr : signal write from bus.
* cs : signal chipselect form bus.

- Outputs :

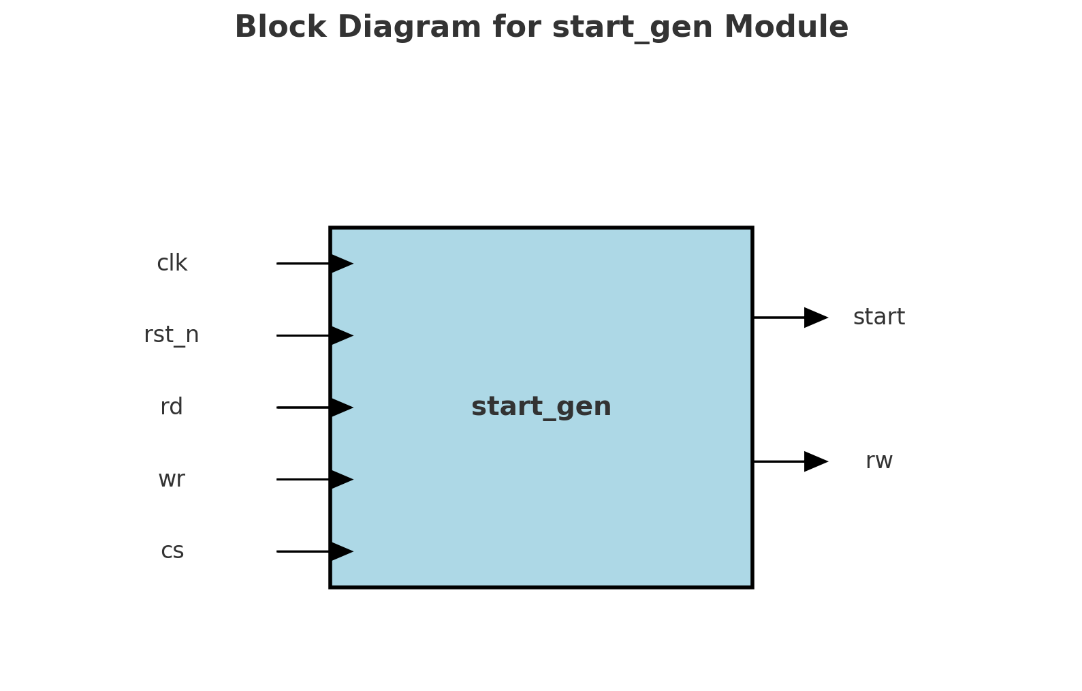
* start : trigger when cs = 1 and rd = 1, or cs = 1 and wr = 1.
* rw : send signal rd or wr to FSM I2C

b. Functional.

- Detect when cs = 1 and rd = 1, or cs = 1 and wr = 1 to start process into FSM I2C to

enable process transfer.

c. Block diagram.



d. Design circuit.

A diagram of a computer circuit

Description automatically generated

e. Timming chart.

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Description automatically generated

3. CLOCK DIVIDE.

a. Inputs / Outputs pin.

c. Functional.

d. Design circuit.

e. Timming chart.

4. FSM I2C MASTER.

a. Inputs / Outputs pin.

c. Functional.

d. Design circuit.

e. Timming chart.

5. FSM I2C SLAVE.