I2C BUS PROTOCOL DESIGN

1. Overview I2C bus protocol

a. Feature.

I2C BUS PROTOCOL

SHIFT

REGISTER

START

GENERATE

I2C\_SLAVE

FSM I2C

b. Block diagram.

TOP MODULE

I2C PROTOCOL BUS

clk\_ex

rst\_n sda\_o

[1:0] address scl

[7:0] idata

[7:0] odata sda\_i

cs

rd

wr

c. Inputs / Outputs pin.

- Input :

* clk\_ex : clock of CPU.
* rst\_n : reset negedge of CPU.
* [1:0] address : 7 bit of address (I2C Slave).
* [7:0] idata : 8 bit of input data.
* cs : chip select posedge.
* rd : read posedge.
* wr : write posedge.
* sda\_i : serial data for read.

- Ouput :

* sda\_0 : serial data for write.
* scl : serial clock.

d. Register specifiaction.

2. START GENERATE.

a. Inputs / Outputs pin.

- Inputs :

* clk : clock internal.
* rst\_n : reset negedge from external.
* rd : signal read from bus.
* wr : signal write from bus.
* cs : signal chipselect form bus.

- Outputs :

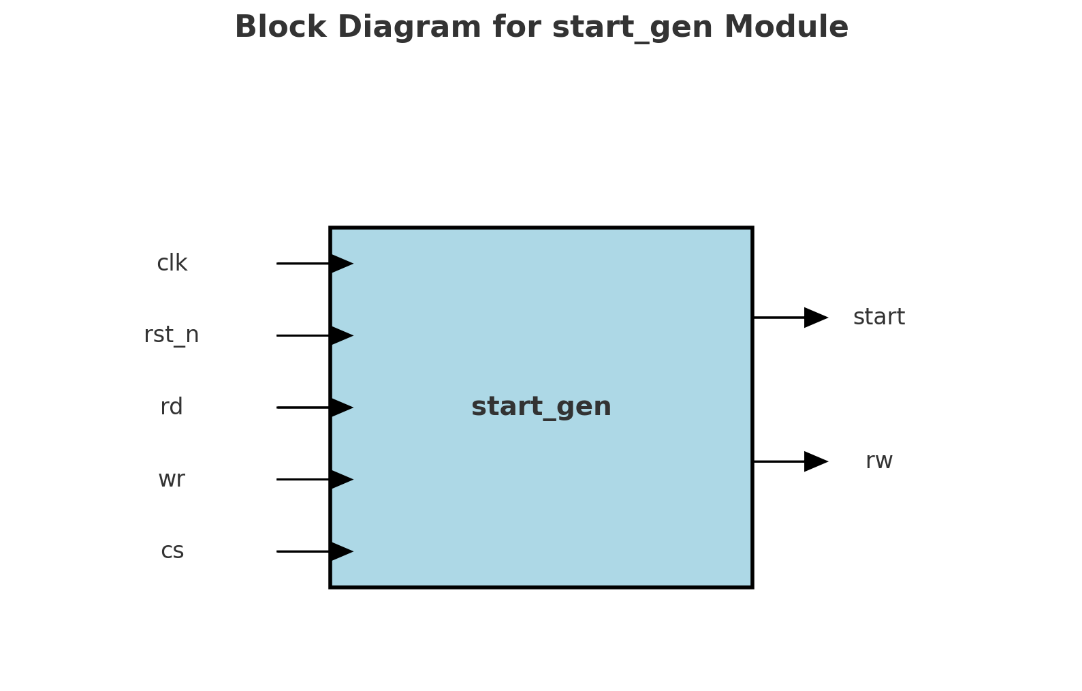
* start : trigger when cs = 1 and rd = 1, or cs = 1 and wr = 1.
* rw : send signal rd or wr to FSM I2C

b. Functional.

- Detect when cs = 1 and rd = 1, or cs = 1 and wr = 1 to start process into FSM I2C to

enable process transfer.

c. Block diagram.



d. Design circuit.

A diagram of a computer circuit

Description automatically generated

e. Timming chart.

A black background with green lines

Description automatically generated

3. FSM I2C.

a. Inputs / Outputs pin.

c. Functional.

d. Design circuit.

e. Timming chart.

4. SHIFT REGISTER.

a. Inputs / Outputs pin.

- Inputs :

* clk : clock internal.
* rst\_n : reset negedge from external.
* Shift\_en : shift enable.
* rw\_en : read or write enable.

+ rw\_en = 0 : write process.

+ rw\_en = 1 : read process.

* [7:0] parallel\_in : data in for write process.
* sda\_in : data in for read process.

- Outputs :

* [7:0] parallel\_out : out data for read process.
* sda\_out : out data for write process.

b. Functional.

- Shift register is used for shift data bits by bits to Slave (from parallel data) and contrast.

c. Block diagram

A diagram of a shift register

Description automatically generated

d. Design circuit.

A diagram of a circuit

Description automatically generated

d. Timming chart.

A computer screen shot of a black and blue screen

Description automatically generated with medium confidence

5. I2C SLAVE.