I2C BUS PROTOCOL DESIGN

1. Overview I2C bus protocol

a. Feature.

I2C BUS PROTOCOL

FSM I2C

SHIFT

REGISTER

START

GENERATE

CLK\_DIV

I2C

b. Block diagram.

TOP MODULE

I2C PROTOCOL BUS

clk\_ex

rst\_n sda\_o

[6:0] address scl

[7:0] idata

[7:0] odata sda\_i

cs\_n

rd\_n

wr\_n

mode

c. Inputs / Outputs pin.

- Input :

* clk\_ex : clock of CPU.
* rst\_en : reset negedge of CPU.
* [6:0] address : 7 bit of address (I2C Slave).
* [7:0] idata : 8 bit of input data.
* cs\_n : chip select negedge.
* rd\_n : read negedge.
* wr\_n : write negedge.
* mode : select low mode (100KHz) or high mode (400KHz).
* sda\_i : serial data for read.

- Ouput :

* sda\_0 : serial data for write.
* scl : serial clock.

d. Register specifiaction.

|  |  |
| --- | --- |
| mode | 0: low mode clk (100KHz)  1: high mode clk (400KHz) |
|  |  |

2. CLK\_DIV I2C.

a. Inputs / Outputs pin.

b. Functional.

c. Design circuit.

d. Timming chart.

3. START GENERATE.

a. Inputs / Outputs pin.

b. Functional.

c. Design circuit.

d. Timming chart.

4. FSM I2C.

a. Inputs / Outputs pin.

b. Functional.

c. Design circuit.

d. Timming chart.

5. SHIFT REGISTER.

a. Inputs / Outputs pin.

b. Functional.

c. Design circuit.

d. Timming chart.